CURRICULUM VITAE

Dr.S.SUBATHRADEVI
Assistant Professor (Sr.Gr.)
Department of Electronics and Communication
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- **Research Area:**
  - VLSI DESIGN
  - DIGITAL SYSTEM DESIGN
  - CAD TOOLS BASED DESIGN
  - DIGITAL COMMUNICATION
  - ANALOG VLSI
  - IMAGE PROCESSING AND ANALYSIS
  - ELECTRICAL NETWORK ANALYSIS AND SYNTHESIS
- **Educational Qualifications:**

Qualification	College/University	Year of completion	Percentage	Class
Ph.D. (specialization)	Information and Communication	Oct. 2010 -Dec.2020	HIGHLY RECOMMENDED	
PG (specialization)	VLSI SYSTEM	July2003- July 2005	6.98 (CGPA)	I st class
UG (specialization)	ECE	1991-1995	68.9%	I st class
HSC	STATE BOARD BIOLOGY,MATHS	1990-91	73.4%	I st class
SSLC	STATE BOARD	1989-90	76%	I st class
Others	NIL	NIL	NIL	NIL

Experience: (chronological order)

Name of Company / Institutions	Designation of Post	From	To	Experience in Year
University College of Engineering BIT campus, Anna University, Tiruchirappalli	Assistant Professor	11-09-2009	Upto the date 30.09.2023	13Y 0M 19D
P.S.N.A. College of Engineering and Technology Dindigul	Senior Lecturer	01-12-2005	28-08-2009	3Y 8M 28D
Saranathan College of Engineering Tiruchirappalli (09-10-2003 to 03-01-2005 study leave- M.Tech.)	Lecturer	16-07-2001	18-10-2005	3Y 0M 10D
M.A.M. college of Engineering	Lecturer	19-04-2001	09-07-2001	2M 21D
Srinivasa Polytechnic, Keeranur, Pudukkottai Dt.	Lecturer	12-06-1996	18-04-2001	4Y 10M 7D
Thirumathi Elizabeth Polytechnic, Perambalur.	Lecturer	05-12-1995	11-06-1996	6M 7D

- **Awards / Honours Received:**

  UGC-NET qualified Ref. No. 8140 NET_DEC.2005 (ELECTRONICS)
  100% RESULT produced recognition received for UG course
  100% RESULT recognition received for PG course

- **Additional / Academic Responsibilities at University:**

  - Class coordinator (Department level)
  - Cultural Coordinator ((Department level)
  - Minutes of meeting in-charge (Department level)
  - Laboratory in charge (Department level)
  - Gold medal distribution committee member in graduation day (Institution level)
  - Logistics member in graduation day in 2012 (Institution level)

Professional Activities at University::

- Internal Examiner for Board Practical Exam
- External Examiner for Board Practical Exam
- Squad member for Board Practical and theory Exam
- Question paper setter for Theory and Practical Exam
- Examiner in paper valuation
- Question paper scrutiny member
- Question paper key preparation member
- Affiliation committee member
- Anna University Representative for Board theory Exam
- Member in steering committee in National conference
- Member in steering committee in International conference
- Judge in National Conference

- **Membership of Scientific and Professional Societies:**

  1. ISTE
  2. IEI

- **Fellowships and Grants received: NIL**
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- **Completed PG/UG Projects:**

  a. Number of PG Projects Completed: 15 Numbers

  b. Number of UG Project Completed: 55 batches

c.

- **Research Guidance (M.S/Ph.D.) (Completed): NIL**

Sl. No	Name of the scholar	Title of the thesis	Year of registration	Date of viva voce
1.				

- **Research Guidance (M.S/Ph.D.) (Ongoing): NIL**

Sl. No	Name of the scholar	Tentative Title of the thesis	Year of registration	Status
1.				

- **Publications:**

Books / book chapters: NIL

a. International Journals:

1. S.Subathardevi, Dr.C.Vennila "Design of four-core Processor with MicroBlaze using Xilinx Tool", **International Journal of Innovative Research in Science, Engineering and Technology,** vol. 4, special issue 6, May 2015.Page No. 606-611. ISSN(Online) : 2319 – 8753, ISSN (Print) : 2347 - 6710 (Vol. 4, Special Issue 6, May 2015, International Journal of Innovative Research in Science Engineering and Technology)

2. S.Subathardevi, Dr.C.Vennila "Modified Reconfigurable Architecture for Binary Array Multiplier with reduced delay", **Indian Journal of Science and Technology''**, Vol.8, Issue 23, Sep.2015. ISSN (Print) : 0974-6846, ISSN (Online) : 0974-5645.(DOI: 10.17485/ijst/2015/v8i23/85354)(Indian Journal of Science and Technology, Vol 8(23), DOI: 10.17485/ijst/2015/v8i23/IPL0887, September 2015)

3. S.Subathardevi, Dr.C.Vennila"Modified Architecture for Distributed Arithmetic with optimized delay using parallel processing", **Indian Journal of Science, Engineering and Technology**. Vol.8, Issue 24, Sep.2015.(**DOI**: 10.17485/ijst/2015/v8i24/82801**)** ISSN (Print) : 0974-6846, ISSN (Online) : 0974-5645. (Indian Journal of Science and Technology, Vol 8(24), IPL0619, September 2015

4. S.Subathardevi, Dr.C.Vennila (18-19 Dec.2015)"Novelty in architecture of ROBDD for the minimization of interconnect delay'', pages 187-191 Published in 2015 International Conference on Control, Instrumentation, Communication and Computational Technologies (ICCICCT) IEEE digital library.DOI:10.1109ICCICCT 2015.7475273. INSPEC Accesion Number: 16005378.

5. S.Subathardevi, Dr.C.Vennila (18-19 Dec.2015) "Survey over on-chip buses for VLSI Architecture with optimized delay for Multiprocessor System design'', pages 372-375 Published in 2015 International Conference on Control, Instrumentation, Communication and Computational Technologies (ICCICCT) IEEE digital library.DOI:10.1109ICCICCT 2015.7475307. INSPEC Accession Number: 16005406.

6. S.Subathardevi,.C.Vennila "An Efficient delay Minimization in System Design using MicroBlaze with BRAM", **International Journal of Research and Reviews in Applied Sciences and Engineering (IJRRASE),** Vol.8, No.1 -2016 pp. 197-203, ISSN2231-0061.

7. S.Subathardevi, C.Vennila, M.Lakshimipraba, B.Logeshwari, S.Malathy, "FFPGA Based Modified Architecture of FFT with Reduced Delay using MACRO", **International Journal of Research and Reviews in Applied Sciences and Engineering (IJRRASE),** Vol.8, No.1 -2016 pp. 204-210, ISSN2231-0061.

8. S.Subathardevi,.C.Vennila, , "Systolic Array Multiplier for Augmenting data centre networks communication links", **International Journal of Cluster Computing – The journal of networks, software tools and applications,** ISSN 1356-7857 **International Journal verlog Springer,** Vol.11, No.4 -2016 pp. 1199-1205.

9. S.Subathardevi,.C.Vennila, , " Delay Optimized Novel Architecture of FIR Filter using Clusterd – Retimed MAC unit Cell for DSP Applications", Natural Publishers The International journal of Applied Mathematics and Information Sciences.

b. <u>International & National Conference Publications:</u>

a. <u>International Conferences:</u>

1. S.Subathardevi, Dr.C.Vennila (29th & 30th April 2015) "Design of four-core Processor with MicroBlaze using Xilinx Tool", **International Conference** on Advances in Communication Technology, Proceedings of MULTICON'15, Muthayammal College of Engineering, Rasipuram.

2. S.Subathardevi, Dr.C.Vennila (25th & 26th July 2015) "Modified Reconfigurable Architecture for Binary Array Multiplier with reduced delay", **International Conference** on ICSCASE2015 Proceedings of ICSCASE 2015, Noorul Islam University, Kanniyakumari.

3. S.Subathardevi, Dr.C.Vennila (25th & 26th July 2015) "Novel Architecture for Distributed Arithmetic with optimized delay using parallel processing",**International Conference** on ICSCASE2015 Proceedings of ICSCASE 2015, Noorul Islam University, Kanniyakumari.

4. S.Subathardevi, Dr.C.Vennila (17th & 18th December2015) "Novelty in architecture of ROBDD for the minimization of interconnect delay'', **International Conference** ICCICCT on Proceedings of ICCICCT-2015, Noorul Islam University, Kanniyakumari. (Journal Published in IEEE Digital Library)

5. S.Subathardevi, Dr.C.Vennila (17th&18th December2015) "Survey over on-chip buses for VLSI Architecture with optimized delay for Multiprocessor System design'', **International Conference** ICCICCT on Proceedings of ICCICCT 2015, Noorul Islam University, Kanniyakumari. (Journal Published in IEEE Digital Library)

6. S.Subathardevi, Dr.C.Vennila, (22nd & 23rd March 2016)"Optimization of interconnect delay in the novel architecture using AXI4'', **International Conference** ICEECE-2016published in Proceedings of ICEECE-2016, Vivekananda College of Engineering for Women, Thiruchengode.

7. S.Subathardevi, Dr.C.Vennila, (22nd & 23rd March 2016) "Optimization of delay in SoC design architecture using Micro Blaze with PLB/AXI4 bus and DDR2'', **International Conference** ICEECE-2016 published in Proceedings of ICEECE-2016, Vivekananda College of Engineering for Women, Thiruchengode.

8. S.Subathardevi, Dr.C.Vennila, R.Vishnupriya, B.Angalaeswari, M.Neethija (21st & 22nd 2016) "Novel Design for BCD adder with minimized delay'', **International Conference** ESD-2016 published in Proceedings of ESD-2016, Avvaiyar College of Engineering for women, Pondicherry. (with ug students)

9. S.Subathardevi, Dr.C.Vennila, M.Lakshmiprabha, B.Logeshwari, S.Malathy "Modified architecture of FFT with reduced interconnect delay for OFDM'', **International Conference** ESD-2016 (17th&18th March 2016) has got selected and published in Proceedings of ESD-2016, Avvaiyar College of Engineering for women, Pondicherry. (with ug students)

10. S.Subathardevi, Dr.C.Vennila, "An efficient delay minimization in System design using Micro Blaze with BRAM'', **International Conference** ESD-2016 (17th&18th March 2016) has got selected and published in Proceedings of ESD-2016, Avvaiyar College of Engineering for women, Pondicherry. (with ug students).

11. S.Subathardevi, Dr.C.Vennila, (2016) "FIR filter", **International Conference** ICEECE 2016 published in Proceedings of ICEECE 2016, Department of ECE and EEE, Anna University BIT Campus, Tiruchirappalli.(Won Best presented Paper award). (with ug students)

12. S.Subathardevi, Dr.C.Vennila, (June 6-June 10, 2016) "Novelty in the Architecture of BDD for the minimization of interconnect delay in System Design", **International Conference** IWCAAM 2016 published in Proceedings of IWCAAM 2016, National Institute of Technology(NIT), Tiruchirappalli.

13. S.Subathardevi, Dr.C.Vennila, (March 31-April 02, 2017) "Delay optimized Matrix Multiplication using 3:2 Compressors for signal processing applications", **International Conference** ICEEE 2017 published in Proceedings of ICEEE 2017,TRP Engineering college, Tiruchirappalli. (with ug students)

14. S.Subathardevi, Dr.C.Vennila, (March 31-April 02, 2017) "Delay optimized BIST for testing and recovery of fault in modeled FPGA components", **International Conference** ICEEE 2017 published in Proceedings of ICEEE 2017,TRP Engineering college, Tiruchirappalli. (with ug students)

b. <u>National Conferences:</u>

Before Joining here

1.Attended a national conference on "Adaptive sensors and Intelligent Systems(NCASIS '08) during November 21-22, 2008 and presented a paper on "Design of High throughput Direct Digital Frequency Synthesizer using DCORDIC " at Sri Ramakrishna Engineering College, Coimbatore.

2. Attended a national conference on "Communication, Networks & Sensor Technology (NCCNS '11) during April 18-19, 2011 and presented a paper on "Delay optimized design of OFDM receiver using DCORDIC " at Hindustan University, Chennai.

AFTER JOINING HERE

1. S.Subathardevi and Dr.C.Vennila (14th March 2015) "Modified Reconfigurable Architecture for Binary Array Multiplier with reduced delay", one day **National Conference** on Advanced Communication, Proceedings of NCACOM 2015, Saranathan College of Engineering, Trichy.

2. S.Subathardevi and Dr.C.Vennila (24th & 25th April 2015) "Modified new Architecture for carry save multiplier with optimizes delay using mirror adder", DRDO sponsored 7th **National Conference** on Signal Processing Communication & VLSI Design, Proceedings of NCSCV'15, Anna University, Regional Center, Coimbatore.

3. S.Subathardevi, Dr.C.Vennila, P.Lavanya, S. Karkuzhali, G. Bavatharani (11th & 12th August 2016) "An Overview on the delay optimized Architecture of FIR filter using FPGA Implementation", TEQIP-II sponsored **National Conference** on Communication and Computing Technologies, published in the Proceedings of NCCCT'16, Anna University –BIT Campus, Tiruchirappalli.

4. S.Subathardevi, Dr.C.Vennila, P.Lavanya, S. Karkuzhali, G. Bavatharani (1st & 2nd September 2016) "Survey on delay constrained FIR filter Architecture",TEQIP-II sponsored **National Conference** on NASCENT Technologies and Signal Processing Communication, published in the Proceedings of NT-SIPCOM'16, Anna University –BIT Campus, Tiruchirappalli.

- **Patents:**

  NIL

- **Sponsored Research Projects: NIL**

Sl.No	Name of the project	Funding agency	Project value (Rs.)	Duration	Status

- **Consultancy Activities: NIL**

Sl.No	Name of the work	Role (PI/Co PI)	Agency	Amount	Duration

- **List of Seminar / Short Term Course /FDP/ Workshop organized:**
  - Workshop (2010), "EMERGING TRENDS ON HIGH END FPGAS", organized by DEPT OF ECE ANNA UNIVERSITY OF TECHNOLOGY TRICHY during 10-12-2010 to 12-12-2010. (3 Days)
  - Workshop (2015), "VLSI DESIGN LAB USING CADENCE TOOL", organized by DEPT OF ECE ANNA UNIVERSITY OF TECHNOLOGY TRICHY during 26-03-2015 to 27-03-2018. (2 Days)
  - SEMINOR (2017), "ADVANCED IMAGE PROCESSING", organized by DEPT OF ECE ANNA UNIVERSITY BIT CAMPUS TRICHY (1 Day)

- **List of Seminar / Short Term Course /FDP/ Workshop attended:**

Before Joining here

a. Workshop (2009), " High Impact Teaching skills- a Dale Carneighe Training Program", organized by PSNA COLLEGE OF Engineering Dindigul during 22-06-2009 to 23-06-2009. (2 Days)

b. Workshop (2008), "ADVANCED ANALOG IC DESIGN", organized by NIT Trichy during 24-09-2008 to24-09-2008. (2 Days)

c. Short Term Course (2007), "Program Title", organized by PSNA College of Engineering and Technology, Dindigul during 22-01-2007 to 2-2-2007. (12 Days)
Workshop (2007), " EC 1404- VLSI Design LAB", organized by Anna University, Trichy during 27-06-2007 to 30-07-2007. (4 Days)

d. Workshop (2003), "Networking,, DSP and Biomedical Engineering", organized by Anna University, GCT Campus, Coimbatore during 06-01-2003 to 07-01-2003. (2 Days)

e. Workshop (2002), "Program Title", organized by Jeyaram College of Engineering, Thuraiyur during 13-06-2018 to14-06-2018. (2 Days)

After Joining here:

a. Workshop (Year), "VLSI DESIGN TECHNIQUES AND APPLICATIONS", organized by DEPARTMENT OF EI DEPT. KLN COLLEGE OF ENGINEERING MADURAI during 03-12-2009 to 04-12-2009. (2 Days)

b. SEMINAR (2010), " TWO DAYS NATIONAL LEVEL SEMINOR ON SPEECH PROCESSING ", organized by .DEPT OF ECE ANNA UNIVERSITY BIT CAMPUS TRICHY during 23-07-2010 to 24-07-2010. (2 Days)

c. Seminar (2010), "SOFTWARE DEFINED RADIO", organized by DEPT OF ECE OXFORD ENGINEERING COLLEGE TRICHY during 27-08-2010 to 28-08-2010. (2 Days)

d. Workshop (2010), " VLSI APPLICATIONS IN HIGHER DATA RATE COMMUNICATIONS AND SIGNAL PROCESSING USING ASIC TOOLS", organized by DEPT OF ECE OXFORD ENGINEERING COLLEGE TRICHY during 12-11-2010 to 13-11-2010. (2 Days)

e. Workshop (2011), "TEACHING METHODOLOGIES", organized by ANNA UNIVERSITY BIT CAMPUS TRICHY on 08/01/2011. (1 Days)

f. Workshop (2011), "RESEARCH METHODOLOGIES", organized by ANNA UNIVERSITY BIT CAMPUS TRICHY on 27/08/2011. (1 Days)

g. Seminar (2011), "Fuzzy Mathematical Modeling and Optimization Techniques ", organized by Anna University of Technology, Tiruchirappalli during 27-07-2011 to 28-11-2011. (2 Days)

h. Seminar (2011), "FUZZY MODELING AND OPTIMIZATION TECHNOLOGIES ", organized by DEPT OF MATHS ANNA UNIERSITY TRICHY during 27-07-2011 to 28-07-2011. (2 Days)

i. Workshop (2011), " DESIGN OPTIMIZATION USING XILINX PLAN AHEAD AND PARTIAL RECONFIGURATION", organized by DEPT OF ECE OXFORD ENGINEERING COLLEGE TRICHY during 16-12-2011 to 17-12-2011. (2 Days)

j. Workshop (2012), " RENESAS 16 BIT MICROCONTROLLERS", organized by DEPT OF ECE ANNA UNIVERSITY BIT CAMPUS TRICHY on 30-05-2012 (1 Days)

k. FDP (2013), "EC2354 VLSI DESGN ", organized by CFD ANNA UNIVERSITY CHENNAI WITH TEQIP during 23-07-2013 to 27-07-2013. (5 Days)

l. Seminar (2013), "Strategic Teaching Quality Management for Technical Teachers ", organized by DEPT OF ECE Anna University BIT Campus, Tiruchirappalli on 16_03_2013. (1 Days)

m. FDP (2013), "SMART TEACHING FOR NET GENERATION (BASIC AND ADVANCED PEDAGOGY", organized by NITTR (MHRD) with TEQIP at ANNA UNIVERSITY BIT CAMPUS TRICHY during 09-12-2013 to 23-12-2013. (15 Days)

n. Workshop (2014), "SYSTEM DESIGN USIG LAB- VIEW", organized by DEPT OF ECE ANNA UNIVERSITY BIT CAMPUS TRICHY during 13-03-2014 to 14-03-2014. (2 Days)

o. Workshop (2014), "EMBEDDED SYSTEM DESIGN FLOW USING VIVADO", organized by VJTI, Mumbai during 10-12-2014 to 11_12_2014. (2 Days)

p. FDP (2014), " THREE DAYS TRAINING PROGRAM ON CADENCE ORCADE SIMULATION PCB DESIGN SOFTWARE", organized by UNIVERSITY COLLEGE OF ENGINEERING VILLUPURAM with FTD AUTOMATION PVT LTD during 12-08-2014 to 3-08-2014. (2 Days)

q. FDP (2015), "NANO TECHNOLOGY APPLICATIONS IN ENGINEERING AND TECHNOLOGY ", organized by DEPT OF PETROCHEMICAL ENGINEERING ANNA UNIVERSITY BIT CAMPUS TRICHY with TEQIP during 06-05-2015 to 19-05-2015. (14 Days)

r. **International Conference** (2016), " IWCAAM 2016 ", International Conference on Mathematical modeling, organized by National Institute of Technology(NIT), Tiruchirappalli during 06_06_2016 to 10_06_2016(5-days).

- **National / International Conferences organized / Participated:**
  - Member in Organising International and National Conference.
  - Participated in International and National Conference.

- **Professional recognitions:** (details like chairperson/member of a committee, reviewer, editor …etc)

(A) Chairperson for conferences / Seminar / Technical symposia:

- **Chair person for National conference**
- **Chair person in Technical symposia**
- **Reviewer in for Inter-National conference**
- **Session Presenter in a Seminor –Network On Chip**
- **Session Presenter in a VLSI workshop - Xilinx**
- **Session Presenter in a VLSI workshop –Cadence Tool**
- **Session Presenter in a FDP –Embedded System**
- **Session Presenter in an Induction Program**

(B) Guest lectures delivered:

- Guest Lecture delivered on Digital System design – Combinational circuits
- Guest Lecture delivered on Digital System design – Sequential circuits.