CURRICULUM VITAE

Mrs.S.Sujitha
Teaching Fellow
Department of Electronics and Communication Engineering
UCE - BIT Campus, Tiruchirappalli 620 024
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- **Research Area:**
  - VLSI Design
  - Image Processing
  - Wireless Communication

- **Educational Qualifications:**

Qualification	College/University	Year of completion	Percentage	Class
Ph.D. (VLSI Design)	Anna University, Chennai.	Pursuing	-	-
PG (M.E - Communication Systems)	Mount Zion College of Engineering and Technology, Pudukottai.	2013	81%	First
UG (B.E - Electronics and Communication Engineering)	Mepco Schlenk Engineering College, Sivakasi	2009	79%	First
Diploma (D.E.E.E - Diploma in Electrical and Electronics Engineering)	Seikalathur Kamatchi Amman Polytechnic College, Manamadurai	2007	96.04%	Frist class with Honours

Experience: (chronological order)

Name of Company / Institutions	Designation of Post	From	To	Experience in Year
University College of Engineering, BIT Campus, Tiruchirappalli	Teaching Fellow	03.01.2022	Till Date	1.7 Years

Mahath Amma Institute of Engineering and Technology	Assistant Professor	05.09.2019	31.12.2021	2.2 Years
University College of Engineering, BIT Campus, Tiruchirappalli	Teaching Fellow	29.01.2015	30.06.2019	4.5 Years
St.Michael College of Engineering and Technology	Assistant Professor	02.09.2019	07.07.2014	10 months

- **Awards / Honours Received:-**
- **Additional / Academic Responsibilities at University:-**
  - Department Exam-Cell Coordinator
  - Department Class Coordinator
- **Membership of Scientific and Professional Societies:-**
- **Fellowships and Grants received:-**
- **Completed PG/UG Projects:**

a. Number of PG Projects Completed: NIL

b. Number of UG Project Completed: 12 batches

- **Research Guidance (M.S/Ph.D.) (Completed):**

Sl. No	Name of the scholar	Title of the thesis	Year of registration	Date of viva voce
1.				

- **Research Guidance (M.S/Ph.D.) (Ongoing):**

Sl. No	Name of the scholar	Tentative Title of the thesis	Year of registration	Status
1.				

- **Publications:**
  - **a. Books / book chapters:-**
  - **b. International Journals:**

1. S.Sujitha (2013), Novel Cache Architecture for Multicore Processor using VLSI, International Journal of Scientific and Engineering Research (ISSN 2229-5518). Vol.4, Issue 06-June 2013.
2. E.Jebamalar Leaveline and S.Sujitha (2022) , Design of Finfet based low power high speed hybrid decoder for SRAM, Microelctronics journal,Elseiver. Article 105499,Vol.126, August 2022 Pg:1-5

c. National Journals:

- **Patents:**

- **Sponsored Research Projects:**

Sl.No	Name of the project	Funding agency	Project value (Rs.)	Duration	Status

- **Consultancy Activities:**

Sl.No	Name of the work	Role (PI/Co PI)	Agency	Amount	Duration

- **List of Seminar / Short Term Course /FDP/ Workshop organized:**
  - Coordinator for TEQIP II sponsored Faculty Development Programme on "Heuristic Approach for Information and Communication Engineering Research problems', Organized by Department of Electronics and Communication Engineering in Bharathidasan Institute of Technology, Tiruchirappalli, held on 15 - 28, June 2016.

- **List of Seminar / Short Term Course /FDP/ Workshop attended:**
  - Attended in Two days Workshop on VLSI Design Lab using Cadence Tool, Organized by Association of Electronics and Communication Engineering Sponsored by TeQIP-II in Bharathidasan Institute of Technology, Tiruchirappalli, held on 26th and 27th, March 2015.
  - Attended in One week Faculty Development Programme EC6501 – Digital Communication(DC-2015), Organized by Department of Electronics and Communication Engineering Sponsored by TeQIP-II in Bharathidasan Institute of Technology, Tiruchirappalli, held on 19th and 25th, June 2015.

- Attended in One Day Faculty Development Programme, Organized by Department of Electronics and Communication Engineering in association with confederation of Indian Industry (CII) in Bharathidasan Institute of Technology, Tiruchirappalli, held on 1st, March 2016.
- Attended in Two-week Faculty Development Programme" Top Tech Trends(T^3) – Driving the future of Information Technology (DFIT), Organized by Department of Computer science and Technology Sponsored by TeQIP-II in Bharathidasan Institute of Technology, Tiruchirappalli, held on 30th June to, 13th July 2016.
- Attended in One Day Faculty Training Programme on "Advanced Communication System", Organized by Department of Electronics and Communication Engineering in Bharathidasan Institute of Technology, Tiruchirappalli, held on 11th, July 2017.
- Attended in One Day National level Workshop on "IoT and Android App Development using MATLAB/Simulink", Organized by Department of Electronics and Communication Engineering in Bharathidasan Institute of Technology, Tiruchirappalli, held on 22th, July 2017.
- Attended in One Day National level Workshop on "Verilog/VHDL coding practice in Xilinx and Quartus Tool", Organized by Department of Electronics and Communication Engineering in K.Ramakrishna College of Technology, Tiruchirappalli, held on 26th , September 2017.
- Attended in One Day Workshop on "Infusing Research attitude through patents and Designs", Organized by PSNA College of Engineering, Dindigul in collaboration with CIPR, Anna University Chennai held on 29th, April 2019.
- Attended in One Day National level Workshop on "Analog Discovery Kit", Organized by Department of Electronics and Communication Engineering in Bharathidasan Institute of Technology, Tiruchirappalli, held on 07th, June 2019.
- Attended one day webinar on "Research Methodology" Organized by Department of Electronics and Communication Engineering in Mount Zion College of Engineering, held on 14th, May 2020.
- Attended one day webinar on "Challenges in Integrating Nano sensors IoT Platform" Organized by Department of Mechanical Information science and Technology in Chennai Institute of Technology Chennai, held on 04th, May 2020.
- Attended Two days International seminar on "Art of Writing scientific articles funding proposal and patents" Organized by Chennai Institute of Technology Chennai, held on 26th & 27th, May 2020.
- Attended one day webinar on "CAD tool for VLSI Design" Organized by Department of Electronics and Communication Engineering in Kamaraj College of Engineering and Technology, held on 13th, June 2020.
- Attended webinar series on "EDA tool for VLSI Applications" Organized by VLSI and Embedded systems SIG in association with IEEE student branch, Department of Electronics and Communication Engineering, Acropolis Institute of technology and research, Indore from 25.6.2020 to 29.6.2020.
- Attended webinar series on "Everyone can do quality Research" Organized by Internal Quality Assurance Cell (IQAC) and Research forum, Knowledge Institute of technology, Salem on 04.07.2020.

- Attended one day webinar on "Business plan to Acquire funding – A Glimpse" Organized by Department of MBA in Gandiapathy Tulsis Jain Engineering College, held on 17th, July 2020.
- Attended Five days Online Short term Course on "VLSI – Physical Design using Cadence Innovus tool" Organized by Department of ECE in St.Joseph College of Engineering, Chennai, held on 20th – 24th July 2020
- Attended three Days Online Workshop on" Academic Writing" Organized by Global Institute of Stastical Solution from 16th to 18th September 2023

➢ **National / International Conferences organized / Participated:**

- S.Sujitha and Anitha.N,(2013) "Low Power and High Speed Cache Architecture for Multicore Processor Using VLSI" International Conference on Advance Computing, Machines and Embedded Technology (ICACT-13), IN JKKN College of Engineering and Technology.
- S.Sujitha(2012) "Design of 1-BIT 6T SRAM cell with CMOS and FInFET using LT Spice" Conference on Intelligent computing and communication Networks(CICCN 2021) in association with computer society of India, in University College of Engineering -BIT Campus, Tiruchirappalli on 26th and 27th February 2021
- S.Sujitha(2021) "Novel Cache Architecture for Multicore Processor Using VLSI" National Conference on Recent Trends in Engineering and Technology in Mount Zion College of Engineering and Technology, Pudukottai on 1st April 2013.

➢ **Professional recognitions:** (details like chairperson/member of a committee, reviewer, editor …etc)

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(A) Chairperson for conferences / Seminar / Technical symposia:

a. Chair Person for the Session in TEQIP II sponsored Two Days National Conference on "Nascent Technologies in Signal Processing and Communication", Organized by Department of Electronics and Communication Engineering in Bharathidasan Institute of Technology, Tiruchirappalli, held on 1 & 2, September 2016.

(B) Guest lectures delivered:

DECLARATION:

I certify that the information furnished above is correct and true to the best of my knowledge and belief.

Signature of the staff member

Head of the Department **Dean**